UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/044,402 | 01/11/2002 | Olivier Menut | 00-GR1-239 | 8917 |

23334 7590 02/14/2005

FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI
& BIANCO P.L.
ONE BOCA COMMERCE CENTER
551 NORTHWEST 77TH STREET, SUITE 111
BOCA RATON, FL 33487

| EXAMINER | |
|---|---|
| BROCK II, PAUL E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/044,402 | MENUT ET AL. | |
| | Examiner | Art Unit | |
| | Paul E. Brock II | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 January 2005 and 01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10,15,17 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15,17 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, 17, 20, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher et al. (USPAT 4942554, Kircher) in view of Jang et al. (USPAT 5637529, Jang).

With regard to claims 1 and 20, Kircher discloses a process for fabricating a semiconductor substrate inherently with a single crystal lattice. Kircher discloses in figures 1 – 5 forming a substrate (1) with a single crystal lattice, the substrate having a top surface with at least one discontinuity in the single crystal lattice therein, whereby the top surface of the substrate has a recess (2) at the discontinuity on the top surface. Kircher does not teach amorphizing the single crystal lattice around a periphery of the recess. Jang teaches in figure 1b amorphizing a single crystal lattice (31) around a periphery of a recess (39). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the amorphizing of Jang in the method of Kircher in order to remove lattice defects, thereby improving yield and productivity of the semiconductor device as stated by Jang in column 1, lines 45 – 50. Kircher discloses in figures 1 – 5 depositing a layer of amorphous material (8)

having the same chemical composition as that of the substrate directly on the underlying structure. It would have been further obvious in the method of Kircher and Jang that the depositing the layer of amorphous material would be performed directly on the structure obtained after amorphizing in order to take advantage of the amorphization of Jang and the amorphous layer of Kircher before any annealing step is performed (see Kircher column 4, lines 13 – 20 and Jang column 2, lines 49 – 60). Kircher discloses in figures 1 – 5 and column 4, lines 13 – 20 thermally annealing the amorphous material so as to be continuous with the single crystal lattice of the substrate.

With regard to claim 2 and 21, Kircher discloses in column 4, lines 6 and 7 planarizing the top surface of the substrate.

With regard to claim 4 and 23, Kircher discloses in column 3, line 44 wherein the step of forming the substrate includes forming the substrate with at least part of the material of silicon.

With regard to claim 17, Kircher and Jang disclose an integrated circuit comprising a silicon substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface and whereby the surface is treated in accordance with the process of claim 1.

3. Claims 3, 5, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher and Jang as applied to claims 1 and 2 above, and further in view of Tan et al. (USPAT 6001706, Tan).

With regard to claims 3 and 22, Kircher teaches a step of planarizing in column 4, lines 6 and 7. Kircher does not teach how the planarization is accomplished. Tan teaches in figure 10a and column 5, lines 53 – 58 wherein a step of planarizing a top surface includes planarizing the top surface by a chemical mechanical polishing. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the chemical mechanical polishing of Tan in the method of Kircher and Jang in order to reliably produce a planar substrate thus improving device yields and device performance.

With regard to claim 5 and 24, Jang teaches in column 2, lines 50 – 60 wherein the step of amorphizing includes amorphizing with a localized ion implantation around the recess by a masking operation.

4. Claims 6 – 10, 15, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher and Jang as applied to claims 1 and 2 above, and further in view of Lill et al. (USPAT 6074954, Lill) and Numazawa et al. (USPAT 6168996, Numazawa).

With regard to claims 6 and 25, Kircher discloses in figures 1 – 5 wherein the step of forming a substrate include the sub-steps of etching a trench, and filling the trench with a fill material so as to form the single-crystal lattice discontinuity. Kircher does not teach depositing first and second layers. Lill teaches in figures 3 – 13b depositing a first layer (6) of a first material and a second layer (8) of a second material in succession on a substrate (2), etching the first layer and an upper portion of a trench fill material (16) so as to form lateral cavities (22) in the second layer in communication with a trench (16) and so as to form the recess at a discontinuity (12). It would have been obvious to one of ordinary skill in the art to use the first

and second layers of Lill in the method of Kircher and Jang in order to provide a mask for the etching of the trench as taught by Lill in column 10, line 56 – column 11, line 37. Kircher, Jang and Lill are silent to removing the second layer. Numazawa teaches in figures 21 and 22 removing a second layer (2b) it would have been obvious to one of ordinary skill in the art at the time of the present invention to use the removing of Numazawa in the method of Kircher, Jang and Lill in order to expose underlying layers for the production of devices that will communicate with the trench.

With regard to claims 7 and 26, Kircher discloses in figure 2 wherein the sub-step of filling of the trench with fill material includes filling the trench with at least part of the fill material of a silicon oxide (4).

With regard to claim 8, Kircher discloses in figure 2 wherein the sub-step of filling of the trench with fill material includes filling at least part of the trench with an insulating fill material.

With regard to claim 9, Lill teaches in figure 4, and column 11, liens 51 – 62 wherein a sub-step of filling the trench is carried out by depositing silicon oxide (10) as a conformal coating. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conformal coating of Lill in order to form a dielectric layer with a defect density low enough for improved performance of DRAM devices.

With regard to claim 10, Numazawa teaches in figure 19 wherein the sub-step of filling of the trench is carried out by thermal oxidation (5a) of the silicon. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thermal oxidation of Numazawa in order to use an efficient and inexpensive means at filling the trench that is proven to form a reliable film.

With regard to claim 15, Jang teaches in figure 1b wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

***Double Patenting***

5. Applicant is advised that should claims 1 – 7 be found allowable, claims 20 – 26 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

***Terminal Disclaimer***

6. The terminal disclaimer filed on January 10, 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of an patents granted on United States Patent Application numbers 10/466,145 and 10/716,249 has been reviewed and is accepted. The terminal disclaimer has been recorded.

***Response to Arguments***

7. Applicant's arguments filed November 1, 2004 and January 10, 2005 have been fully considered but they are not persuasive.

8. With regard to applicant's argument that "Kircher expressly teaches depositing the amorphous layer 8 on an isolating silicon oxide layer 7, and not directly on the substrate 5," it should be noted that this characterization of Kircher is not consistent with the disclosure of Kircher. Figure 5 of Kircher clearly shows the deposition of amorphous layer 8 directly on, and in contact with substrate 1. Further, figure 5 of Kircher clearly shows that the amorphous layer is also directly deposited on the fill material 5. Therefore, applicant's arguments are not persuasive and the rejection is proper.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II